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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,161	02/13/2002	Masatoshi Yano	DP-850 US	4727
21254	7590	11/30/2004	EXAMINER	
MCGINN & GIBB, PLLC 8321 OLD COURTHOUSE ROAD SUITE 200 VIENNA, VA 22182-3817			BUTLER, DENNIS	
			ART UNIT	PAPER NUMBER
			2115	

DATE MAILED: 11/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/073,161	MASATOSHI YANO
Examiner	Art Unit	
Dennis M. Butler	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 13 February 2002.

2a) This action is **FINAL**. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) Claim(s) _____ is/are allowed.
6) Claim(s) 1-20 is/are rejected.
7) Claim(s) _____ is/are objected to.
8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 01072004.

4) Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ .

5) Notice of Informal Patent Application (PTO-152)

6) Other: ____ .

1. This action is in response to the application filed on February 13, 2002. Claims 1-20 are pending.
2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Coppola et al., U. S. Patent 5,216,357.

Per claim 1:

A) Coppola et al teach the following claimed items:

1. a control section for controlling the terminal device with microprocessor 24 of figure 2;
2. a first real time clock (RTC) that is built in the control section with clock 26 of figure 2 and at column 5, lines 51-55;
3. a second real time clock (RTC) outside the control section with clock 46 of figure 2 and at column 5, lines 61-65;
4. the control section obtaining information from the first RTC when the terminal is in a first (normal) operation mode at column 5, lines 21-37 and 51-55;

5. the control section obtaining information from the second RTC when the terminal is in a second (power failure) operation mode at column 6, lines 4-27.

Per claims 2-10:

Coppola describes that clock 46 is directly connected to microprocessor 24 with the two lines shown directly connecting these two devices in figure 2. Coppola describes that clock 46 is connected to microprocessor 24 via a functional device (the two lines shown connecting these two devices and the interface circuitry) in figure 2. Coppola describes that clock 46 is built in a functional device connected to microprocessor 24 as shown in figure 2. Clock 46 is inherently built in a circuit board, a chip or some other type of device. Coppola describes transferring information from the second RTC to the first RTC, restoring the first RTC and thereafter the control section obtains information from the first RTC at column 6, lines 28-39. Coppola describes that the control section is powered by main DC power supply 15 and the second RTC (clock 46) is powered by battery 48 at column 6, lines 1-19. Coppola describes the information includes time and date information at column 5, lines 65-68. Coppola describes that the first mode is a normal operating mode and the second mode is a recovery from failure mode at column 5, lines 21-37 and at column 6, lines 4-39. Coppola describes that the control section is a microprocessor built in the terminal with microprocessor 24 of figure 2.

Per claim 11:

A) Coppola et al teach the following claimed items:

1. a mode judgment step for judging whether the terminal is in a first (normal) operation mode or a second (power failure) operation mode with power line outage detector 50 of figure 2, with element 62 of figure 4, with element 92 of figure 5 and at column 6, lines 4-27;
2. a control section for controlling the terminal device with microprocessor 24 of figure 2;
3. a first real time clock (RTC) that is built in the control section with clock 26 of figure 2 and at column 5, lines 51-55;
4. a second real time clock (RTC) outside the control section with clock 46 of figure 2 and at column 5, lines 61-65;
5. a first information obtaining step in which the control section obtains information from the first RTC when the terminal is in a first (normal) operation mode at column 5, lines 21-37 and 51-55;
6. a second information obtaining step in which the control section obtains information from the second RTC when the terminal is in a second (power failure) operation mode at column 6, lines 4-27.

Per claims 12-20:

Coppola describes that clock 46 is directly connected to microprocessor 24 with the two lines shown directly connecting these two devices in figure 2. Coppola describes that clock 46 is connected to microprocessor 24 via a functional device (the two lines shown connecting these two devices and the interface circuitry) in figure 2. Coppola describes that clock 46 is built in a functional device connected

to microprocessor 24 as shown in figure 2. Clock 46 is inherently built in a circuit board, a chip or some other type of device. Coppola describes transferring information from the second RTC to the first RTC, restoring the first RTC and thereafter the control section obtains information from the first RTC at column 6, lines 28-39. Coppola describes that the control section is powered by main DC power supply 15 and the second RTC (clock 46) is powered by battery 48 at column 6, lines 1-19. Coppola describes the information includes time and date information at column 5, lines 65-68. Coppola describes that the first mode is a normal operating mode and the second mode is a recovery from failure mode at column 5, lines 21-37 and at column 6, lines 4-39. Coppola describes that the control section is a microprocessor built in the terminal with microprocessor 24 of figure 2.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is 571-272-3663. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.
For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dennis M. Butler

Dennis M. Butler
Primary Examiner
Art Unit 2115